REMARKS

In response to the Office Action mailed February 15, 2005, the Applicants request entry of the amendments to the Claims as set forth above, and consideration of the following remarks. In the Office Action the Examiner objected to the Brief Description of the Drawings and rejected all of the pending claims, namely, Claims 1-22.

The Examiner rejected Claims 1, 4, 7, 10, 13, 16, 21, and 22 under 35 U.S.C. § 102 based on U.S. Patent Number 4,410,990 issued to Wilkinson.

The Examiner rejected Claims 2, 5, 8, 11, 15, 18, and 20 under 35 U.S.C. § 103 based on U.S. Patent Number 4,410,990 issued to Wilkinson in view of U.S. Patent Number 6,269,096 issued to Hann.

The Examiner also rejected Claims 3, 6, 9, 12, 14, 17, and 19 under 35 U.S.C. § 103 based on U.S. Patent Number 4,410,990 issued to Wilkinson in view of U.S. Patent Number 5,459,723 issued to Thor.

The Applicants request review of the remarks which following in view of the claim amendments and reconsideration as to the allowability of the claims.

Objection to Specification

The Examiner objected to the Brief Description of the Drawing by asserting that the Description at pages 5 and 6 mentions Figures 4 and 5 two times. Applicants have reviewed the text at pages 5 and 6 and the description of Figure 4 and 5 are only listed once. Applicants acknowledge that the description of Figure 6 cross-references Figure 4 and that the description of Figure 7 cross-references Figure 5, but this is entirely proper and not prohibited under the rules. Applicants request reconsideration by the Examiner.

Rejection based on U.S. Patent Number 4,410,990 issued to Wilkinson.

The Examiner rejected Claims 1, 4, 7, 10, 13, 16, 21, and 22 under 35 U.S.C. § 102 based on U.S. Patent Number 4,410,990 issued to Wilkinson.

The Examiner rejected Claims 1, 4, 7, and 10 on the same rationale. In this rejection, the Examiner asserted that the Wilkinson reference taught all of the elements and limitations of these claims. As way of summary, Wilkinson is directed to recovery of framing data. (Column 1, lines 9-10, Column 1, lines 45-46). In contrast, the present invention is directed to improving the speed of scrambling and descrambling of data. As a result, the Wilkinson reference is directed to a different method and apparatus.

Stated another way, recovering framing information is not the same as scrambling and de-scrambling of data. Recovering framing information may occur before or after scrambling, but it is not the process of scrambling and de-scrambling data. The Wilkinson reference reinforces this view, namely, ". . . framing, this latter term meaning identification of which bits in the stream of binary data form the required blocks of bits representing the control and information signal." (Column 1, lines 21-24)

Scrambling, on the other hand, is the random arrangement of bits (1's and 0's) in an irregular fashion. (see generally Column 3, lines 30-56). In particular, as stated in the Wilkinson reference at column 3, lines 54-56:

> Some form of scrambling may also be applied to the information bits, but this is not relevant to the invention and will not thereby described herein.

Therefore, Applicants submit that the Wilkinson reference cited by the Examiner is not relevant to the present application, which deals with a faster method and apparatus for scrambling and descrambling of data based on parallel processing.

Working from this understanding of the differences between the Wilkinson reference and the present application, Claims 1, 4, 7, 10, 13, 16, 21, and 22 which were rejected under 35 U.S.C. § 102 based on U.S. Patent Number 4,410,990 issued to Wilkinson, all contain a limitation requiring parallel processing and are written in the context of parallel processing of the data for either scrambling or descrambling. The applicants have amended Claims 13 and 16 as shown above to more clearly describe the claimed subject matter.

Support for the parallel processing feature is provided in Figure 6, which shows multiple XOR logic elements 2023, 2007, 2031, 2015. In addition, support is found at page 4 of the Summary section of the application, a portion of which is reproduced below:

> The **parallel processing** SD system of the present invention stores serially transmitted input bits and a copy of recently scrambled and serially transmitted input bits, in registers of appropriate sizes, **performing the XOR SD operation in parallel** on a plurality of bits, and then serially transmitting the output of the XOR operation.
>
> **Parallel scrambling substantially accelerates the data processing rate**, and has the added advantage that an integral number of bytes may be processed at a time. Clearly, the higher the number of data bits processed in parallel, the higher the data processing rate will be. (Present Application, emphases added.)

The passages cited by the Examiner do not teach this limitation nor would such a variation be obvious to one of ordinary skill in the art reading the Wilkinson reference. Based on electronic searching, the only passage in the Wilkinson reference that uses the term parallel is found at column 4, line 64 through column 5, line 6 and reads as follows:

> To identify the framing, therefore, the fifteen bits held in each of the shift registers 10, 11, 12 and 13 are continuously supplied in parallel to respective 15-bit comparators 14, 15, 16 and 17 to which the parity scrambling code is also supplied in parallel

> from a read only memory 18. On identifying a perfect or near-perfect match between the fifteen bits held in one of the shift registers 10, 11, 12 or 13 and the parity scrambling code, the relevant comparator 14, 15, 16 or 17 supplies a signal to a frame lock circuit 18 to indicate that the incoming bit received by the receiver 2 is the last bit of a frame. (Wilkinson reference)

In this passage, it is the bits and the scrambling code that are supplied in parallel to comparators. This passage does not describe parallel processing for scrambling and descrambling as claimed.

In support of this position, Figure 2 of the Wilkinson reference shows only a single logic element (EX-OR) 5 in the transmitter 1 and a single logic element (EX-OR) 20 in the receiver 2. Thus, it would not be possible for the system of the Wilkinson reference to perform the parallel processing as claimed in the present application, because it contains only a single EX-OR element.

Applicants request allowance of independent Claims 1, 4, 7, 10, 13, and 16. The remaining dependent Claims, which depend from these independent claims, are submitted as also allowable due to their dependency from an allowable base claim.

Rejection Under 35 U.S.C. § 103 based on Wilkinson in view of Hann

The Examiner also rejected Claims 2, 5, 8, 11, 15, 18, and 20 under 35 U.S.C. § 103 based on U.S. Patent Number 4,410,990 issued to Wilkinson in view of U.S. Patent Number 6,269,096 issued to Hann. All of these claims are dependent claims, namely, Claim 2 depends from Claim 1; Claim 5 depends from Claim 4; Claim 8 depends from Claim 7; Claim 11 depends from Claim 10; Claims 15 and 18 depend from Claim 13; Claim 20 depends from Claim 16. The Applicants submit that these dependent claims are also allowable, because these

claims depend from allowable independent claims. The independent claims are allowable for the reasons stated above.

In addition, the Hann reference cited by the Examiner does not teach parallel processing for scrambling and descrambling. The Hann reference is directed to receiving and transmitting blocks for ATM cell delineation. Thus, the system and method of the Hann reference is not related to the invention as claimed and does not teach the elements missing from the Wilkinson reference. The Hann reference is cited by the Examiner for teaching a 45 bit scrambling bit sequence and an electronic search of the Hann reference does not reveal the term "parallel".

Rejection Under 35 U.S.C. § 103 based on Wilkinson in view of Thor

The Examiner rejected Claims 3, 6, 9, 12, 14, 17, and 19 under 35 U.S.C. § 103 based on U.S. Patent Number 4,410,990 issued to Wilkinson in view of U.S. Patent Number 5,459,723 issued to Thor. All of these claims are dependent claims, namely, Claim 3 depends from Claim 1; Claim 6 depends from Claim 4; Claim 9 depends from Claim 7; Claim 12 depends from Claim 10; Claim 14 depends from Claim 13; Claims 17 and 19 depends from Claim 16. The Applicants submits that these dependent claims are also allowable, because these claims depend from allowable independent claims. The independent claims are allowable for the reasons stated above.

In addition, the Thor reference cited by the Examiner does not teach parallel processing for scrambling and descrambling. The Thor reference is directed to packet management device and is simply not related to the invention as claimed. This reference is cited by the Examiner for teaching use of 32 bits for the HDLC transmitter and an electronic search of the Thor reference does not reveal the term "parallel".

SUMMARY

Applicants assert that Claims 1-22 are in a condition for allowance and respectfully requests a notice as to the same. If any matters remain outstanding, the Examiner is invited to contact the undersigned by telephone.

Respectfully submitted,

Dated: 6/15/05 By: C. Miller

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